

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/821,723	MERRY ET AL.	
		Examiner	Art Unit	Page 1 of 1
		Patricia A. George	1765	

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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**FOREIGN PATENT DOCUMENTS**

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	Q					
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	S					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Leverd et al. (Wsi/Poly-Si gate Stack etching for advanced dRAM applications (1999 IEEE/SEMI Advanced Semiconductor manufacturing Conference and Workshop; Sept. 8-10. 1999; Boston, MA, USA).
	V	Wolf et al (Silicon Processing for the VLSI Era; Vol. 1; 1986; Lattice Press)
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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